What is claimed is:

1. A PLL circuit comprising:

an oscillation circuit that generates an oscillation signal with an oscillation frequency based on a supplied voltage;

a frequency divider that divides the frequency of the generated oscillation signal based on a predetermined frequency dividing number to generate a comparison signal;

a phase comparator that generates a phase difference signal indicative of a phase difference between the generated comparison signal and a reference signal;

a low-pass filter that generates a voltage signal formed as a direct current from the generated phase difference signal and that supplies the voltage signal to the oscillation circuit;

a controlling unit that switches at a predetermined timing to enable/disable the phase difference signal supplied from the phase comparator to the low pass filter; and

a resistor element that is disposed between a predetermined potential and a signal line for supplying the phase difference signal from the phase comparator to the low pass filter,

when the phase difference signal is enabled, the oscillation circuit performing oscillation operation based on the voltage signal corresponding to the phase difference signal,

when the phase difference signal is disabled, the low pass filter being supplied with the predetermined potential through

the resistor element to allow the oscillation circuit to perform oscillation operation based on the voltage signal generated depending on the supplied predetermined potential.

2. The PLL circuit of claim 1, wherein

a charge pump is disposed between the phase comparator and the low-pass filter to convert the level of the phase difference signal, and wherein

when a control signal is supplied to disable the phase difference signal, the controlling unit performs control to set the output level of the charge pump to high impedance.

3. The PLL circuit of claim 1 or 2, wherein

the resistance value of the resistor element is set depending on the extent of spreading the power spectrum correlated with the oscillation frequency of the oscillation signal.

4. The PLL circuit of any one of claims 1, 2, and 3, wherein

the period for which the phase difference signal is disabled is set depending on the extent of attenuating the peak level of the power spectrum correlated with the oscillation frequency of the oscillation signal.

5. The PLL circuit of any one of claims 1, 2, and 3, wherein

the period for which the phase difference signal is

disabled is set depending on the extent of spreading the power spectrum correlated with the oscillation frequency of the oscillation signal.